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How to perform safely As the number of users decreases the server load will also decrease which will allow for the servers to work properly and hopefully have a lot less downtime in the future. Also, be sure to check the "DDoS" warnings when accessing the server which will always be there if the server is under duress. In high speed applications such as those in video and graphics applications, the timing of the clock signal to the external components is of utmost importance. The components require a clock signal to function properly and inaccuracies in the clock signal propagation delay or skewing of the clock signal can result in inaccurate data being provided. In addition, the longer the propagation delay of the clock signal the more jitter and uncertainty is introduced. A delay locked loop ("DLL") circuit is typically employed in a data recovery circuit to generate an accurate clock signal, as well as an accurate set up time, and hold time by adjusting the delay of the clock signal. FIG. 1 depicts a conventional DLL circuit 102. DLL circuit 102 receives a clock signal, CLK, and a feedback clock signal, FBCLK. DLL circuit 102 delays FBCLK and provides the delayed signal as a clock signal, CLK_DLL. The timing relationship between CLK and CLK_DLL is dependent on the delay characteristics of DLL circuit 102. The delay model for DLL circuit 102 is determined by the characteristics of the transistors and other components that comprise DLL circuit 102. Any undesired delay in the setup time or hold time of CLK or CLK_DLL adversely affects the data recovery. As a result, DLL circuit 102 is typically calibrated for a particular process, voltage, and temperature ("PVT") condition to insure that the timing relationships between CLK and CLK_DLL are accurate. This calibration process, however, has several drawbacks. DLL circuit 102 typically has a variable delay which is a function of the process, voltage and temperature (PVT) conditions. Different PVT conditions result in different delays. In addition, different PVT conditions result in different delay models for DLL circuit 102, which results in different delay characteristics. It is also noted that DLL circuit 102 can include a current mode logic ("CML") block which introduces process and voltage (PVD) dependent delays in DLL circuit 102. Once DLL circuit 102 is calibrated for a particular PVT condition,

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